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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/670,416	09/25/2003	Shao-Pin Ru	7257/71150	7920

7590 11/01/2005

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EXAMINER	
PHAN, THIEM D	
ART UNIT	**PAPER NUMBER**
3729	

DATE MAILED: 11/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/670,416	RU, SHAO-PIN	
	Examiner	Art Unit	
	Tim Phan	3729	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) *11-13* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election of Group I, Claims 1-10, filed on 9/14/05 is acknowledged.

The Restriction mailed on 8/12/05 has been carefully reviewed and is held to be proper. Applicant did not distinctly and specifically point out any logical error in the Restriction Requirement. Moreover, due to the lack of traversal on the merits, Applicant's election of Group I, claims 1-10, has been treated as an election without traverse.

Accordingly, Claims 11-13 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected Group, there being no allowable generic or linking claim.

The Restriction filed on 8/12/05 is hereby **made Final**.

Applicant is required to cancel these nonelected claims (11-13) or take other appropriate action.

An Office Action on the merits of Claims 1-10 now follows.

Title

2. The following title is suggested: "Method of Fabricating a Thin Film Integrated Circuit with Thick Film Resistor".

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 2 and 5 are rejected under 35 U.S.C. 102(b) as being anticipated by Brown et al (US 5,994,997).

As applied to claim 1, Brown et al teach a method of forming thick film resistors (Fig. 3, 110) integrated with a thin film circuit (Fig. 3, 28), by first creating multiple thick film resistors (Fig. 3, 110; col. 1, lines 21 & 22) on a substrate (Fig. 3, 112), and then creating a thin film circuit portion (Fig. 3, 28) over the substrate to be interconnected with the thick film resistors.

As applied to claim 2, Brown et al teach that the fabrication process of integrating thick film resistor components with a thin film circuit portion on a printed circuit board involves a first

phase process of forming the thick film resistors comprising the acts of:

- forming conductive electrodes (Fig. 3, 22 & 24) for thick film resistors, wherein pairs of electrodes are formed at predetermined positions over a substrate (Fig. 3, 112) and each electrode pair acts as the end terminals of the thick film resistors;
- forming a resistive coating (Fig. 3, 126) for thick film resistors in between the electrode pairs to finish a thick film resistor;
- forming a passivation or dielectric layer (Fig. 3, 114; col. 5, line 66) over the thick film resistors that were heat-dried (Col. 1, lines 27-34), where a lower temperature process is used to form a dielectric layer to protect the thick film resistors.

As applied to claim 5, Brown et al teach that the formation of the conductive electrodes and the resistive coating for the thick film resistors, and the passivation layer all require a high temperature sintering or baking process to fuse all solid material (Col. 1, lines 27-34) after finishing the coating.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Brown et al.

As applied to claim 6, Brown et al teach a method of forming thick film resistors, which reads on applicants' claimed invention, except for the screen printing technique of forming the conductive electrodes and the passivation layer.

It is mere matter of design choice to apply screen printing technique of forming the conductive electrodes and the passivation layer, since it was known in the art that the electrodes can be made by plating, laminating and etching techniques (Col. 5, lines 6-11) and a screen printing technique of the formation of the resistive coating (Col. 5, lines 15-25) for the thick film resistors followed by the formation of the dielectric or passivation layer and it appears that the invention would perform equally well with many different techniques.

7. Claims 3, 4, 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown et al in view of Jo et al (US 6,881,679).

As applied to claims 3 and 4, Brown et al teach a method of forming thick film resistors, including the thin film circuit (Col. 5, lines 5-13) comprising:

- forming a copper layer (Fig. 3, 28; col. 4, 61) over the substrate (Fig. 3, 112) with the thick film resistors (Fig. 3, 126);
- attaching a dry film or photoresist (Col. 4, lines 62 & 63) over the copper layer;

- exposing and developing (Col. 4, lines 63-65) , wherein the dry film is placed over the circuit portion as a photomask to shield against exposure light, and a circuit pattern appears on the dry film after developing;
- electroplating (Col. 4, line 61; col. 5, line 10) the thin film circuit for interconnections to form a copper plated circuit;
- removing remnants of the dry film and excess portions of the copper layer over the substrate to finish the formation of the thin film circuit (Fig. 3, 28), using lithographic etching or other means (Col. 5, lines 5-13).

Jo et al teach a method of fabricating an electrode or circuit of copper and titanium with an etching solution in order to have low resistivity (Col. 1, lines 41-43) and improved etching rate (Col. 4, line 6) of the circuit.

It would be obvious to one of ordinary skill in the art at the time the invention was made to combine the two teachings by applying the electrode or circuit of copper/titanium with an etching solution, as taught by Jo et al, to the method of manufacturing thick film resistor , electrode and circuit of Brown et al in order to ease the manufacturing process to have low resistivity and improved etching rate of the electrode/terminal and conductive circuit.

As applied to claims 9 and 10, Brown et al teach the sputtering or spraying process to obtain the electroless copper flash (Col. 4, line 49) for forming the conductive circuit layer as disclosed by USPN 5,162,144 (Col. 4, lines 50-59).

8. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown et al in view of Lauffer et al (US 5,027,253).

As applied to claims 7 and 8, Brown et al teach a method of forming thick film resistors, which reads on applicants' claimed invention.

Lauffer et al teach a process of fabricating printed circuit boards with embedded component (Fig. 2, 141) using several passivation or dielectric layers (Fig. 2, 201 or Fig.3, 305c) and conductive electrode layers (Fig. 2, 123 or Fig. 3, 311a; col. 11, line 60) of thickness about 3 to100 microns in order to increase the packing density of the package.

It would be obvious to one of ordinary skill in the art at the time the invention was made to combine the two teachings by applying the process of fabricating the PCB, as taught by Lauffer et al, to the method of forming thick film resistors by Brown et al in order to increase the packing density of the package.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicants' disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tim Phan whose telephone number is 571-272-4568. The examiner can normally be reached on M - F, 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Peter Vo can be reached on 571-272-4690. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application lnformation Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have any questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tim Phan
Examiner
Art Unit 3729

A. DEXTER TUGBANG
PRIMARY EXAMINER

tp
October 28, 2005